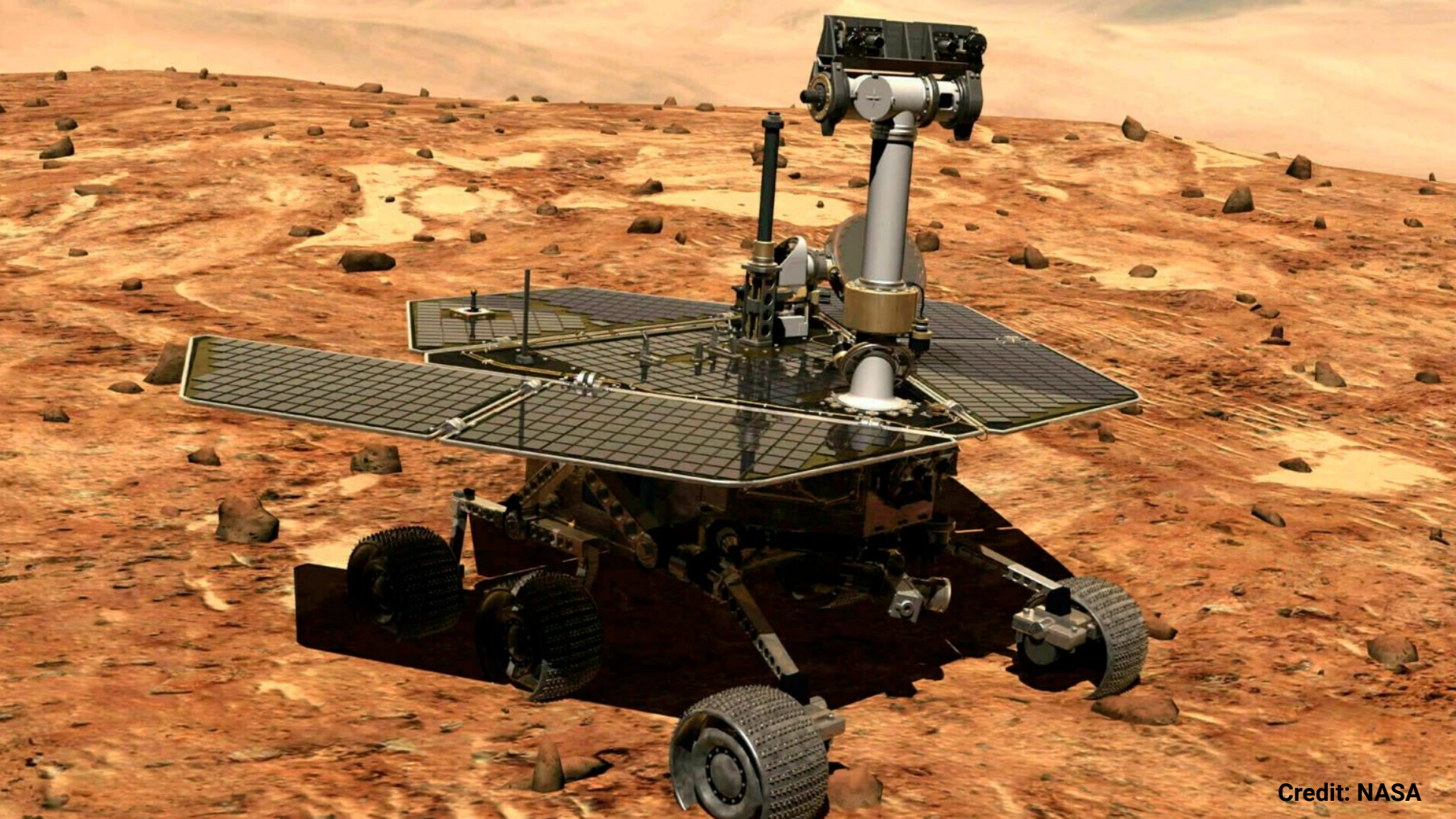


# What is a clock?

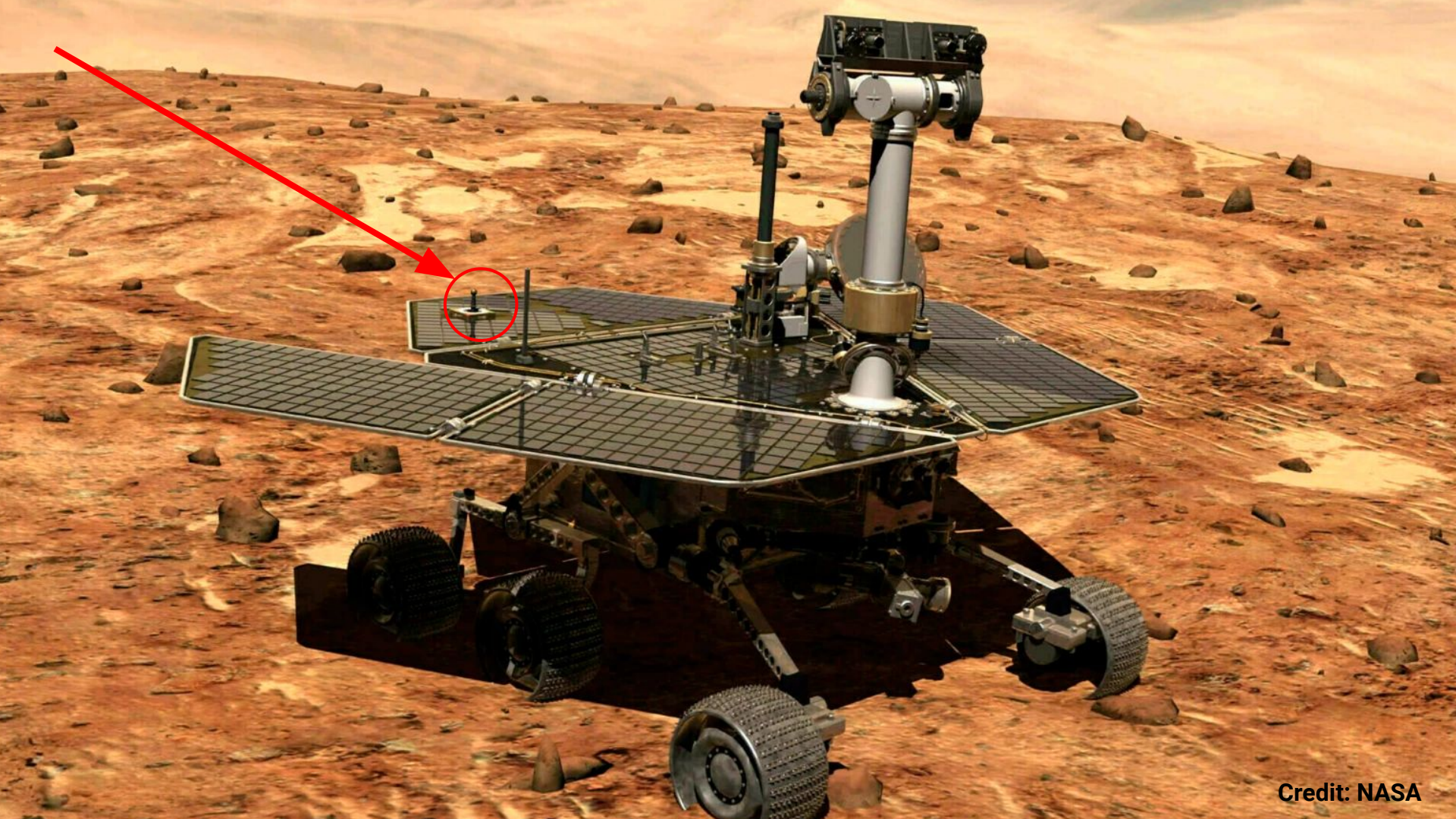
A close-up, 3D-rendered yellow pen nib pointing towards the bottom right of the slide.

**Patrik Fältström**  
**Technical Director and Head of Security**





Credit: NASA



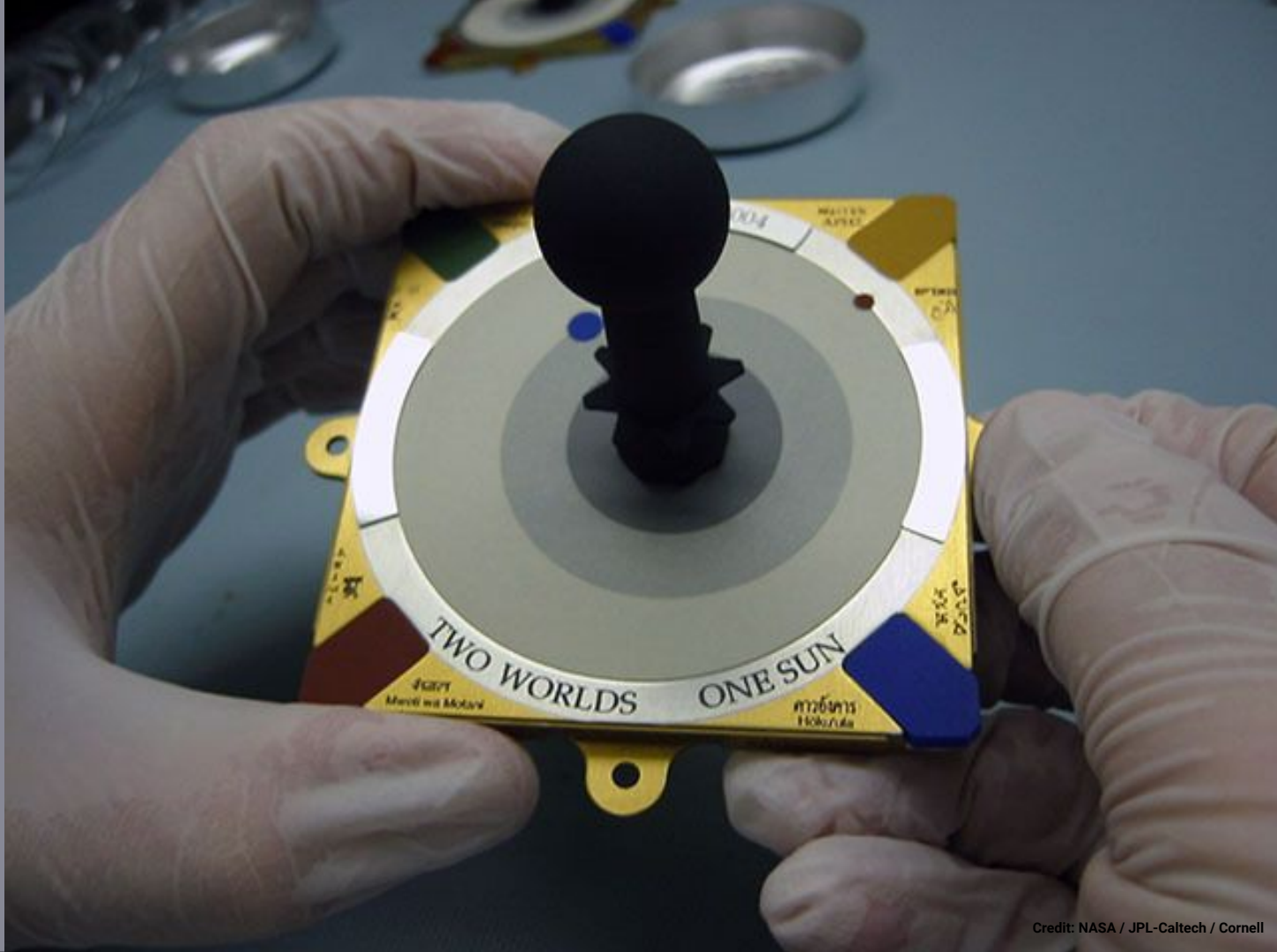
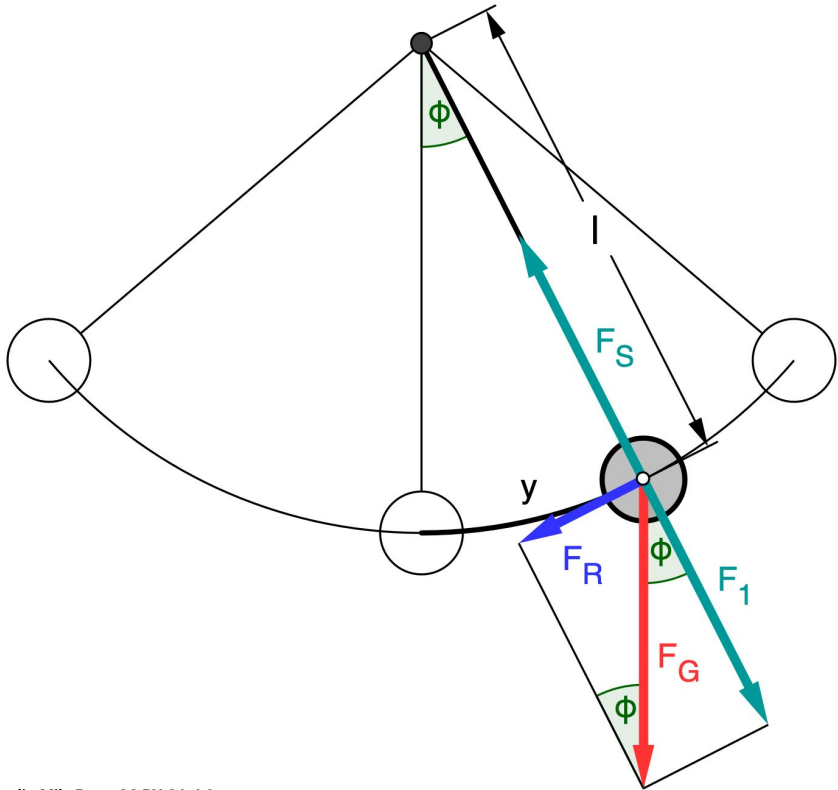
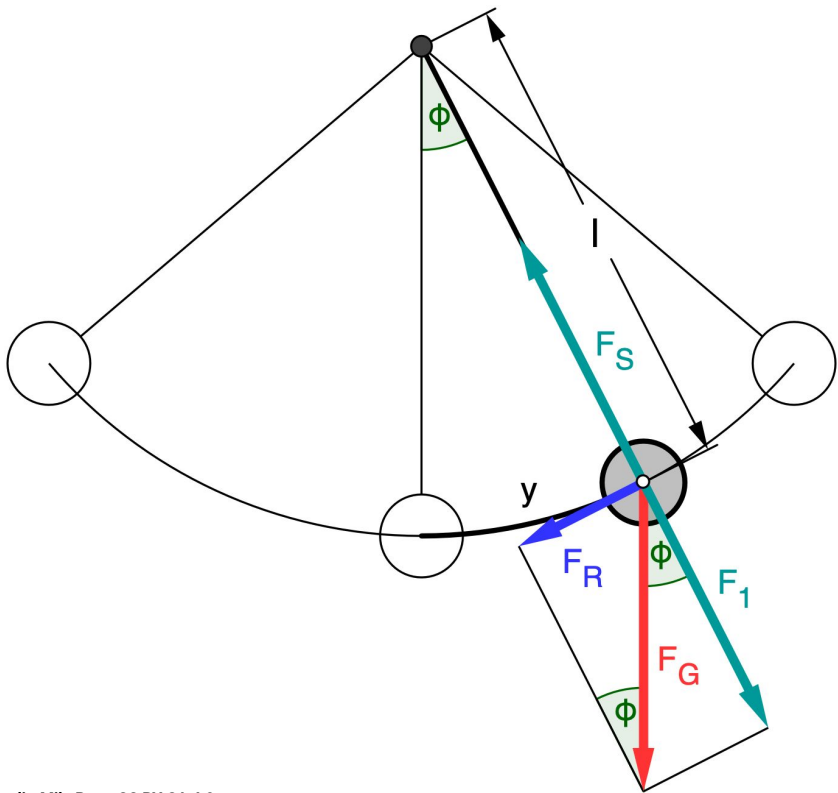




Foto: Rikard Ågren CC BY-SA 4.0



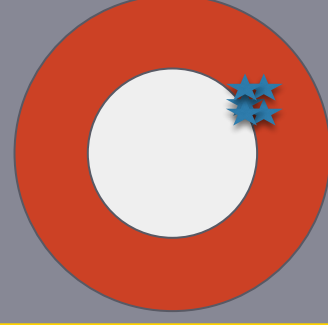
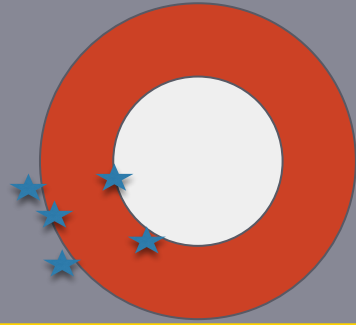
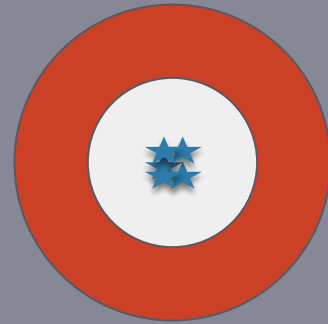
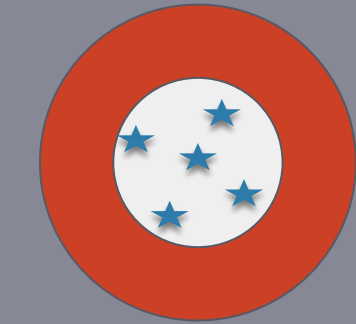




Correctness

High

Low



Low

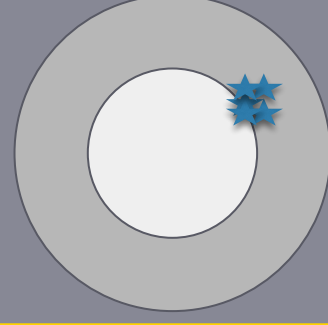
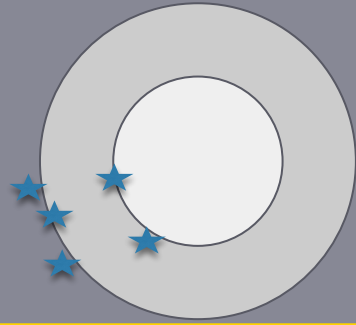
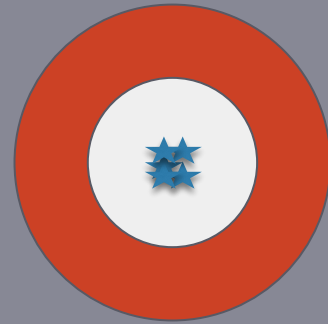
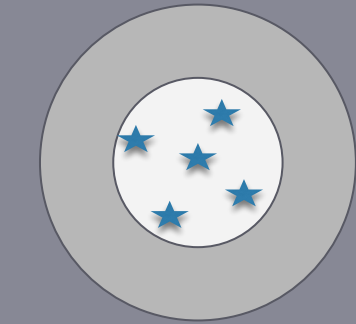
High

Precision

Correctness

High

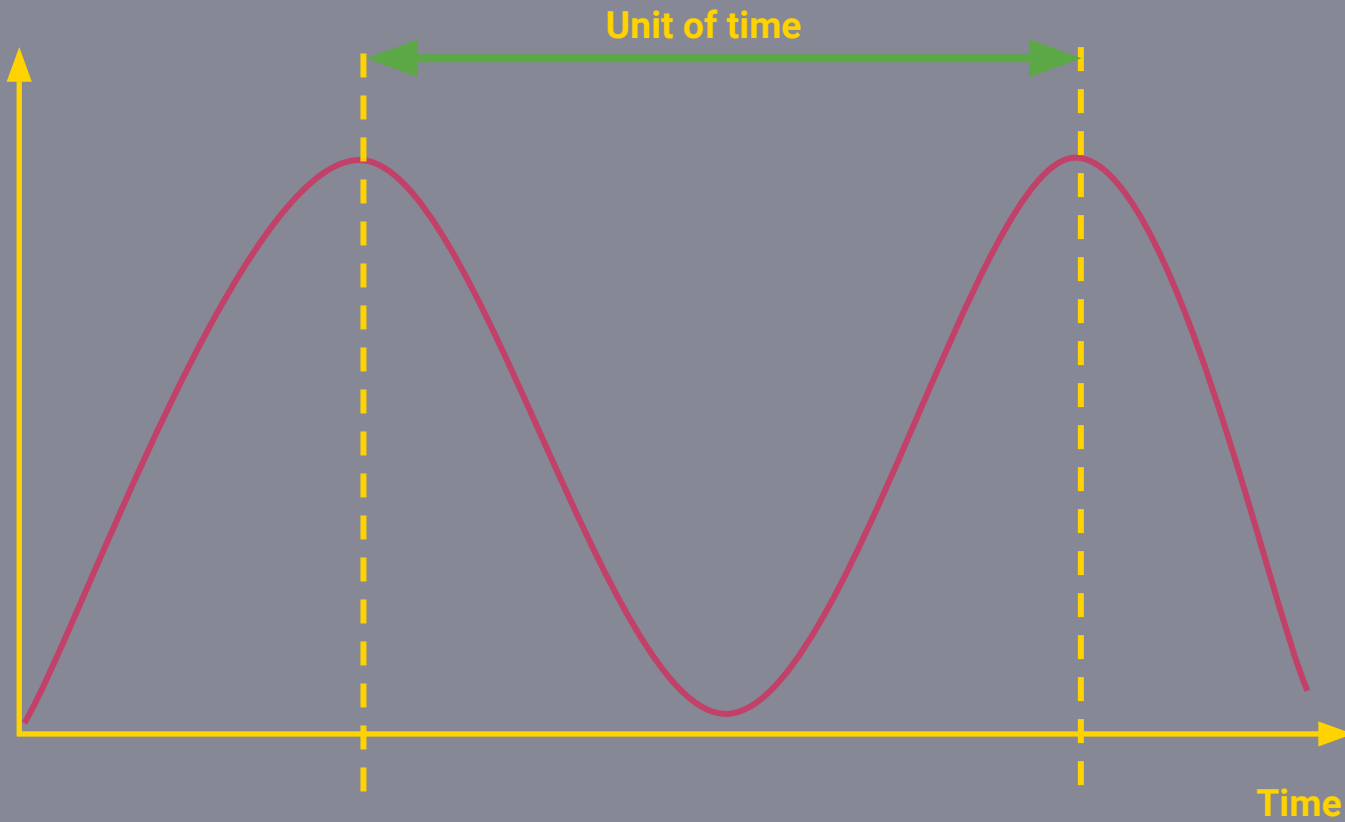
Low



Low

High

Precision



THE INTERNATIONAL MERIDIAN CONFERENCE,  
WASHINGTON, 1884.

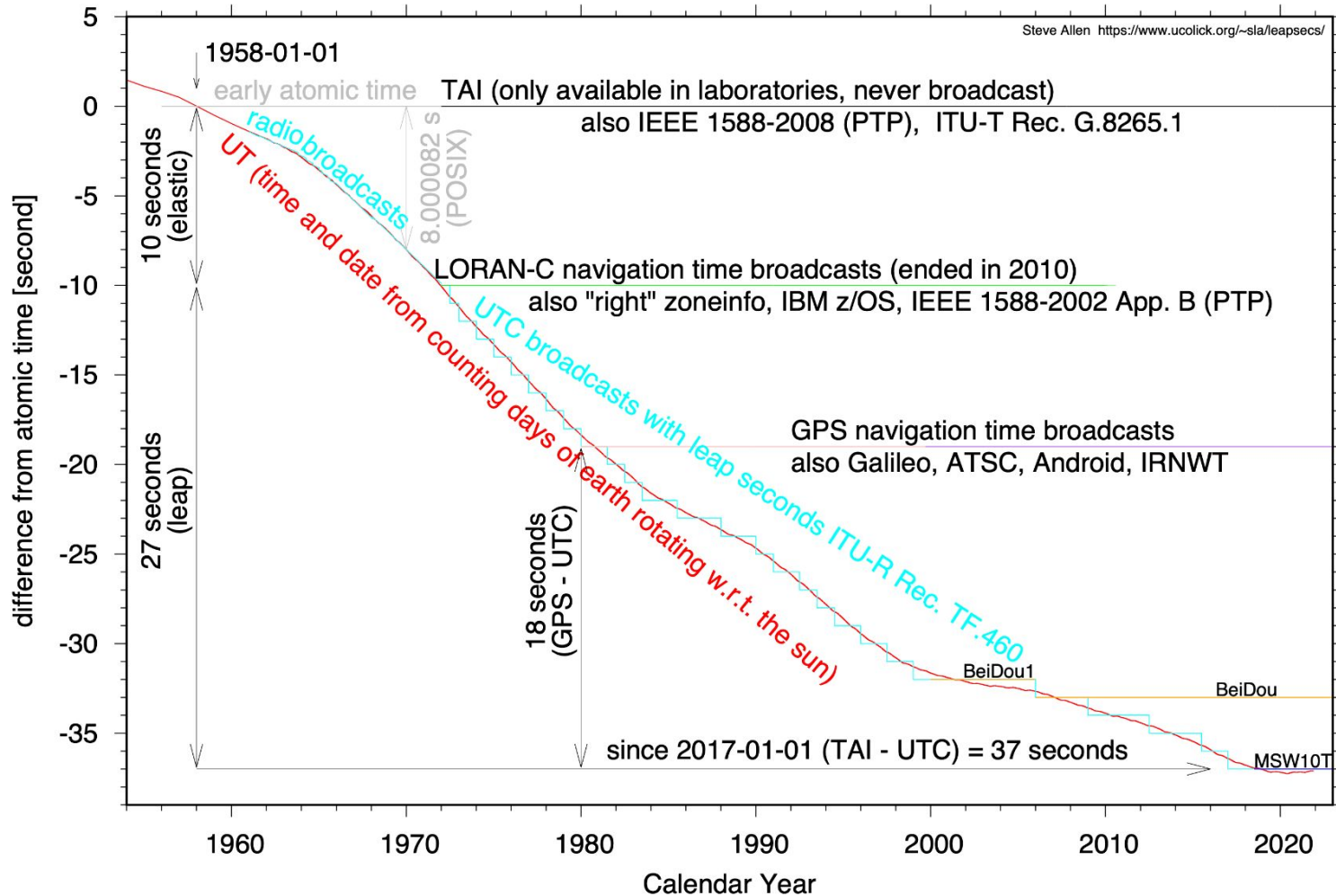


Born von ALVENLESEN, Minister of Sweden.	M. de J. GALVAN, Minister of San Domingo.	A. LEFAVRE, Chief-Deputé of France.	LI-GEN STRACHEY, Secretary, Great Britain.	M. JANSSEN, Secretary, Belgium.	Admiral C. R. P. RODERS, President, Great Britain.	DR. L. CIRILS, Secretary, Brazil.	G. H. de WEGHERLIN, Minister of Netherlands.	Born von SCHÄFFER, Minister of Austria.
MR. HINCKELDEYN, Gronawa.	J. VALLERA, Minister of Spain.	A. M. SOYFELD, France.	DR. J. C. ADAMS, Great Britain.	DR. J. O. EVANS, Great Britain.	W. F. PEDDICK, Deputé Secretary U. S.	SUSTEM EFFENDI, Turkey.	Count FORESTA, Italy.	
DR. C. FRIEDL, Ministry of Antwerp.	L. M. BATHURST, Ireland.	CLEVELAND ABBE, United States.	J. de KOLODRNOFF, Russia.	C. de STROVE, Russian Ministry.	Major-General STEBENTZ, Russia.	General W. T. SAMSON, United States.	A. ANGIANO, Italy.	A. L. ADEE, Acting Deputy Minister of U. S.
JUAN PASTORIN, Spain.	F. V. GONZALEZ, Spain.	A. S. TIPPER, Ireland.	Count LEWENHaupt, Minister of Saxe-Coburg. Jura.	M. A. BATES, Minister of Saxe-Coburg. Jura.	M. M. ROCK, Ireland.	L. ARNOLD, Commandant of Argentine.	Count J. STEWART, Commandant of Argentine.	F. R. MARCEAU, French Geographer.
			J. F. ECHEVERRIA, Uruguay.	W. D. ALEXANDER, Hawaii.				

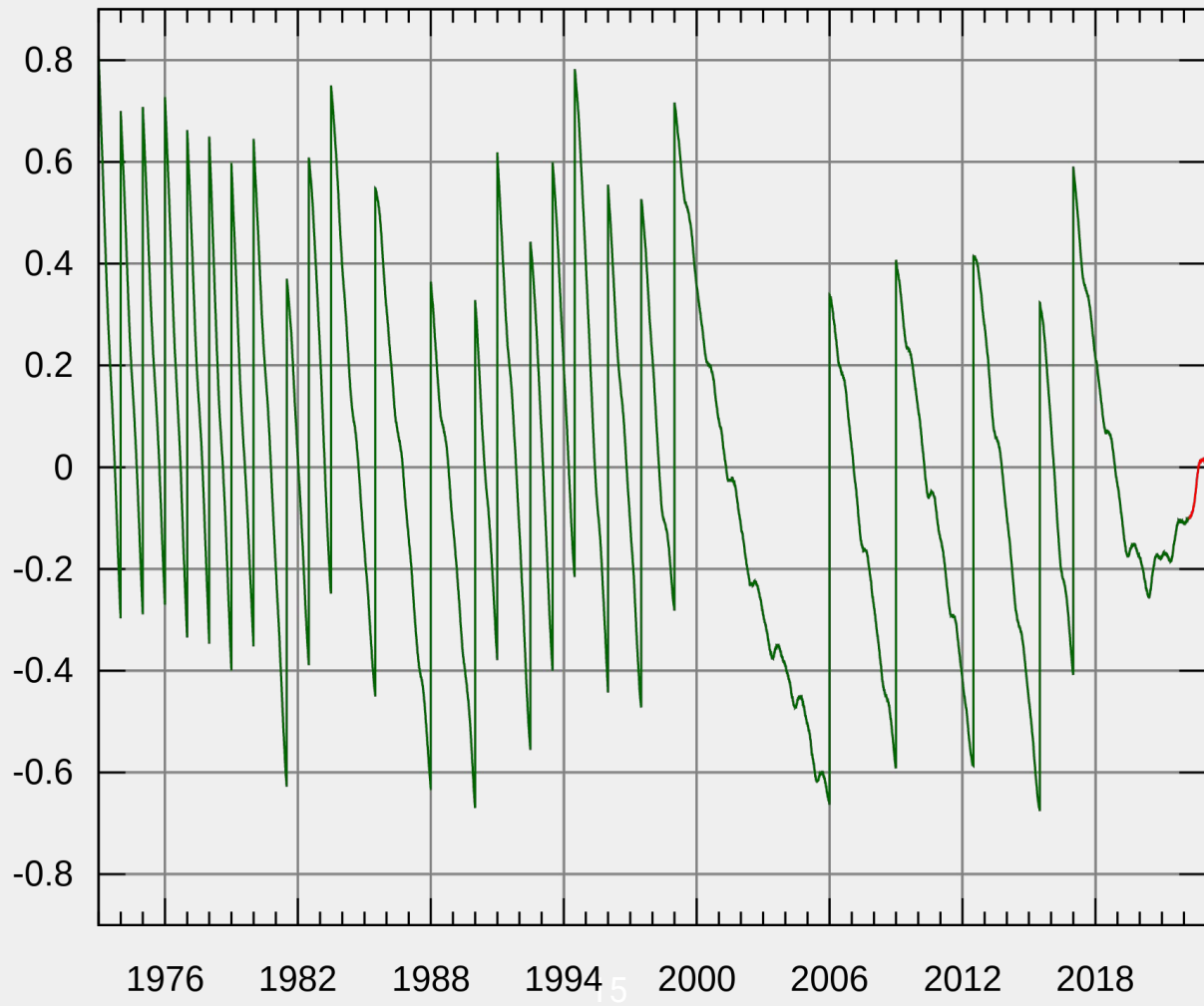
# Timescales

- UT1 - Universal time is defined by the Earth's rotation, with adjustment to polar wandering
- TAI - International Atomic Time is defined as the weighted average of the time kept by about 200 atomic clocks in over 50 national laboratories worldwide
  - TAI-UT1 was approximately 0 on January 1, 1958
- UTC - Coordinated Universal Time is a multiple number of SI seconds
  - UTC differs from TAI by an integral number of seconds
  - When needed, leap seconds are introduced in UTC to keep the difference between UTC and UT1 less than 0.9 s
  - UTC was introduced in 1972
- GPS - Global Positioning System, does not have leap seconds
  - GPS is 19 second difference from TAI


# Time scales since the cesium atomic frequency standard



UT1 - UTC

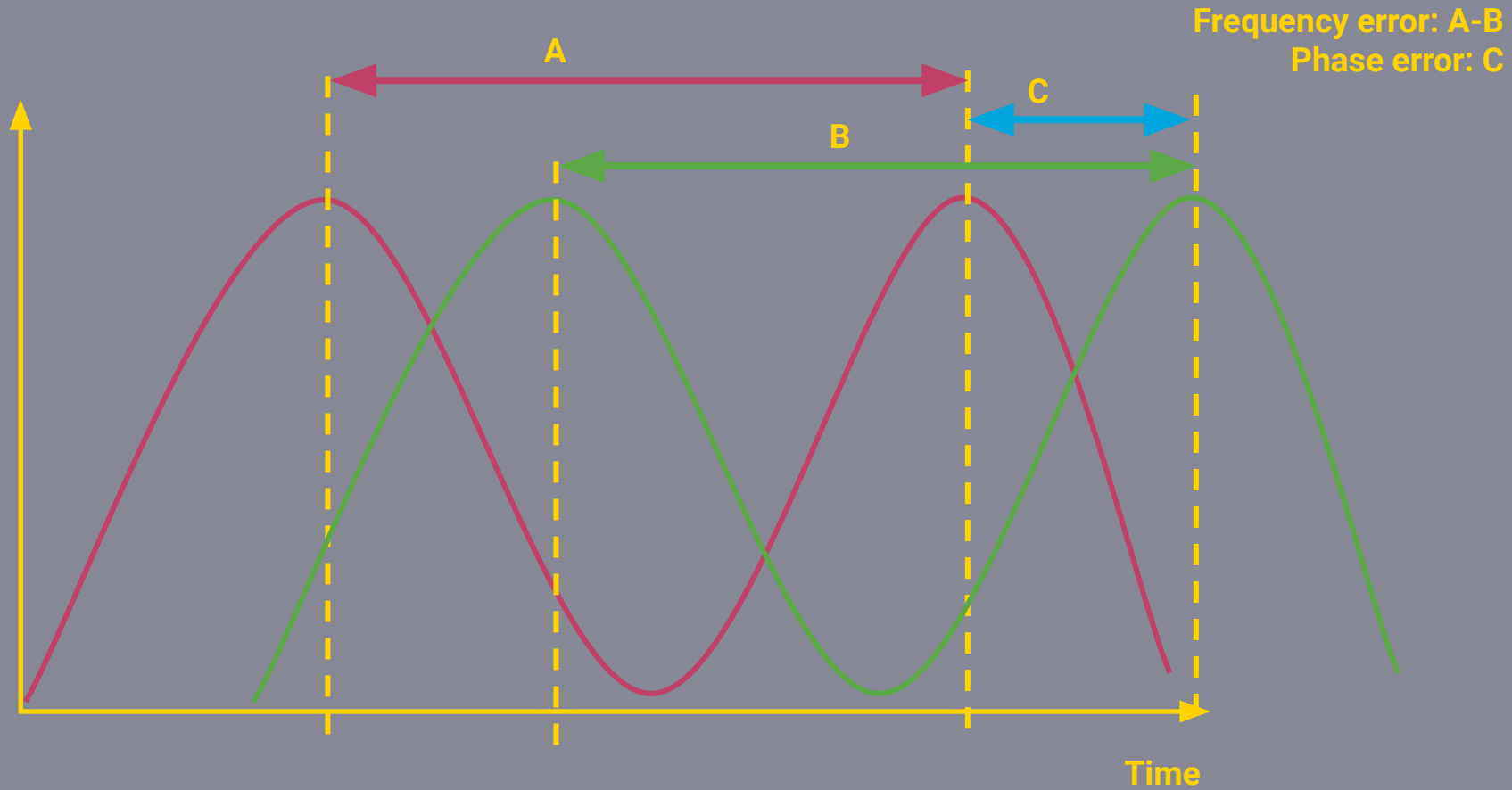


# Leap Seconds

- POSIX definition of time is simple:
  - 86400 times number of days since 00:00:00 January 1 1970 UTC
  - Within a day number of seconds since midnight
- Understand leap seconds 
- GPS have similar issues
  - Signal:
    - Weeks since Jan 6, 1980
    - Milliseconds within a week
  - Week is 10 bit counter
  - Wraps every  $2^{10}$  weeks (~20 years)
  - Did wrap April 7, 2019

UTC	POSIX Time
2016-12-31 23:59:59.0	1483228799.0
2016-12-31 23:59:59.5	1483228799.5
2016-12-31 23:59:60.0	<b>1483228800.0</b>
2016-12-31 23:59:60.5	<b>1483228800.5</b>
2017-01-01 00:00:00.0	<b>1483228800.0</b>
2017-01-01 00:00:00.5	<b>1483228800.5</b>
2017-01-01 00:00:01.0	1483228801.0
2017-01-01 00:00:01.5	1483228801.5



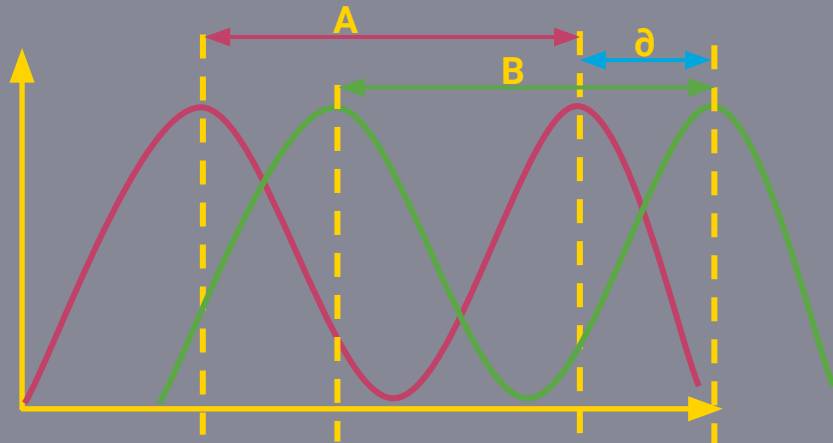




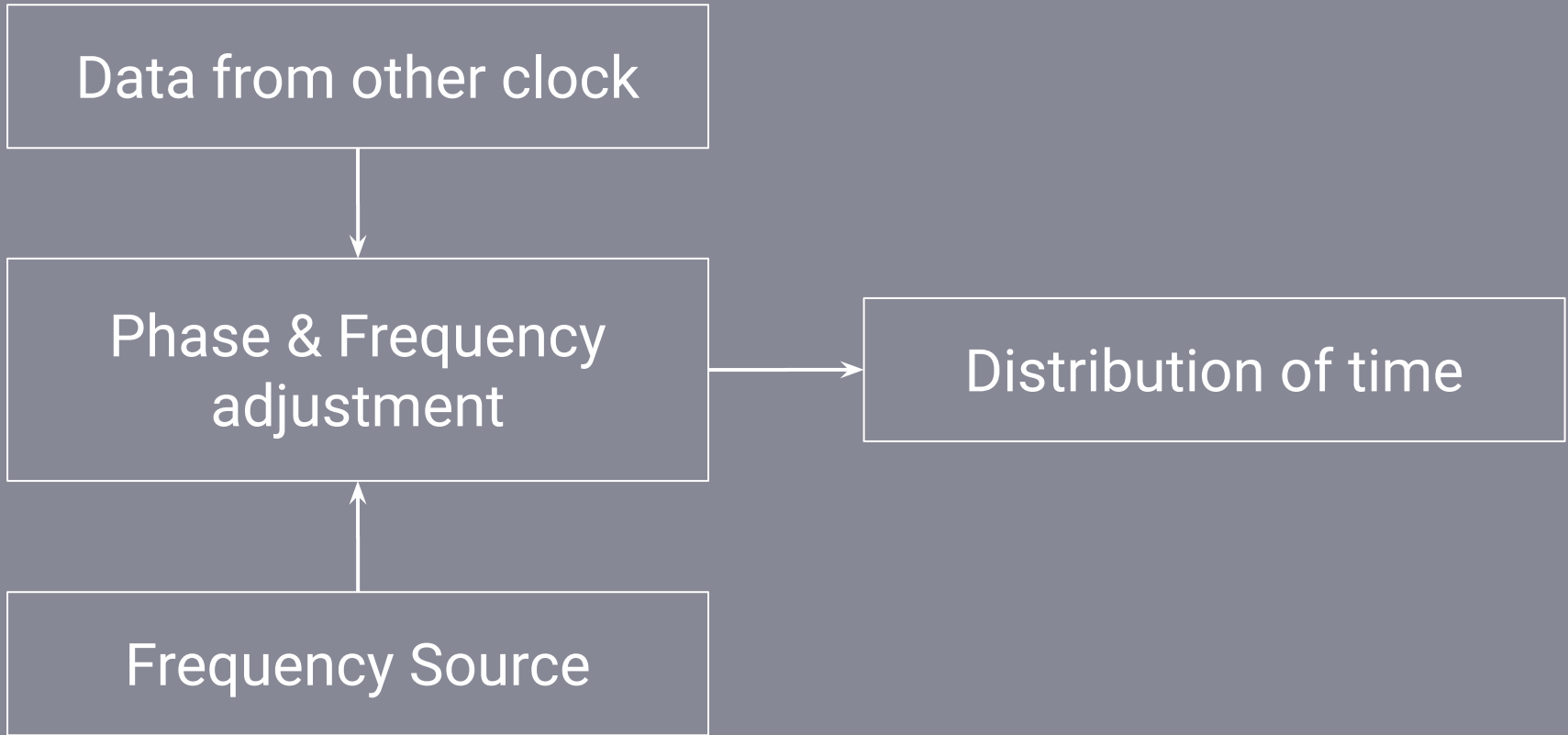
Source: A

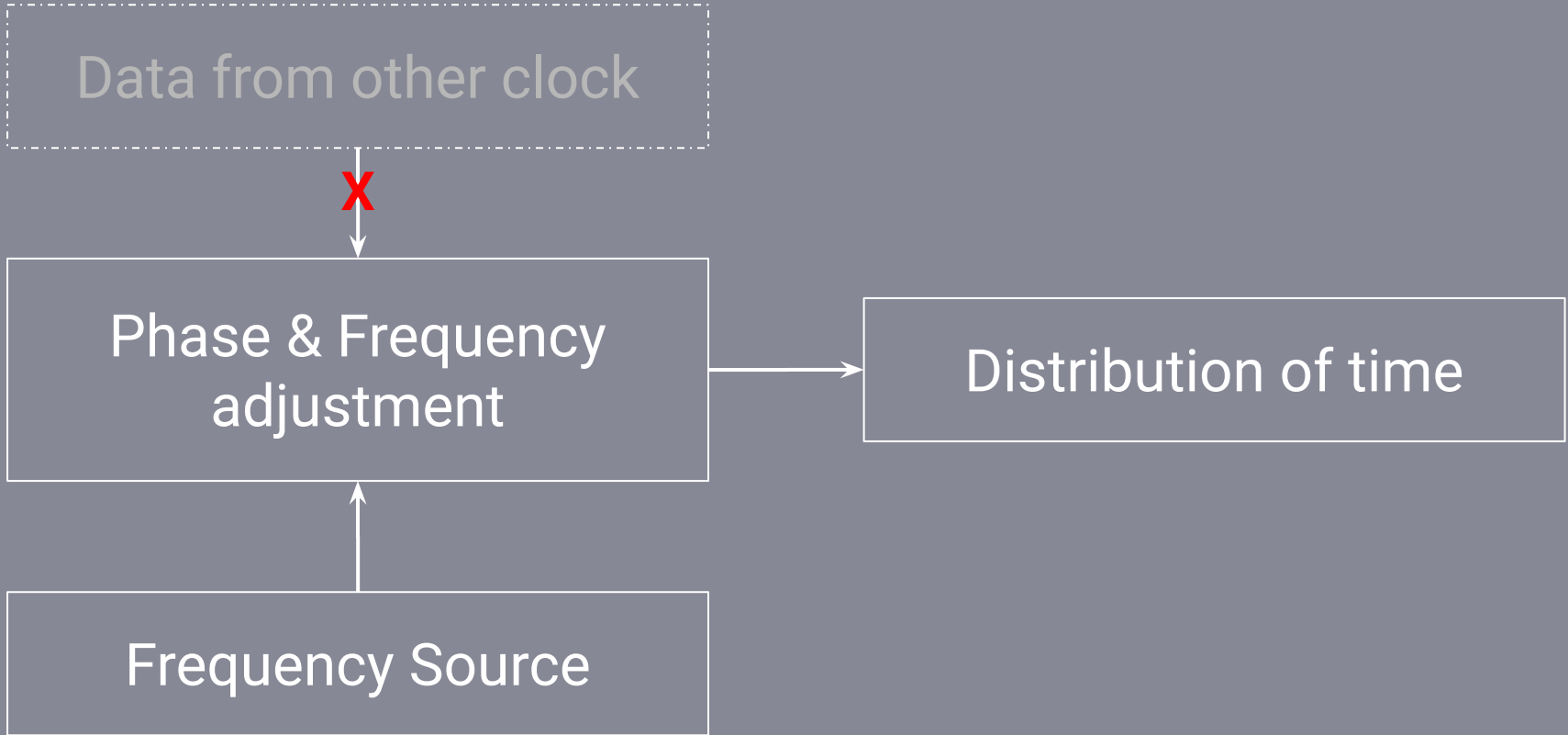


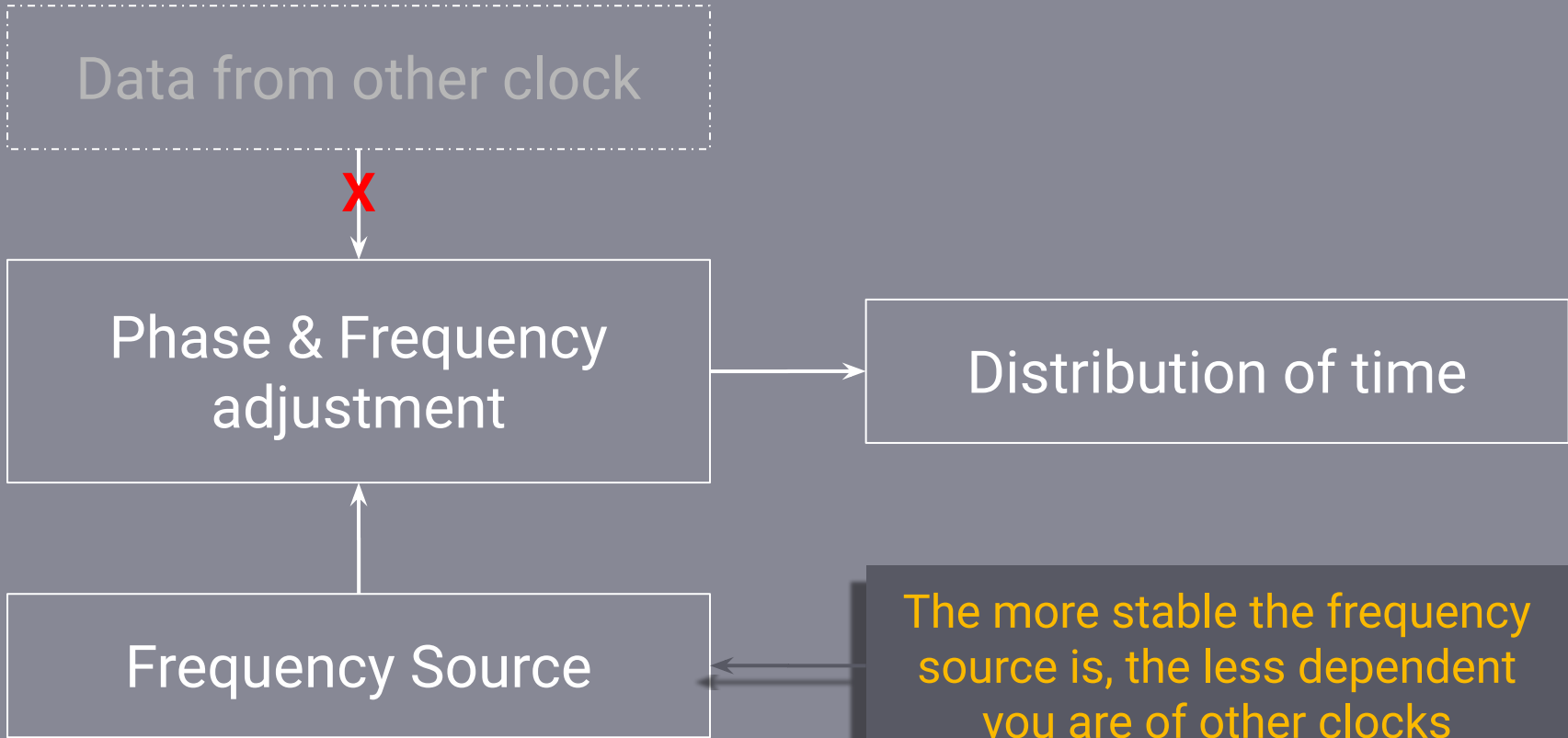
Target: B

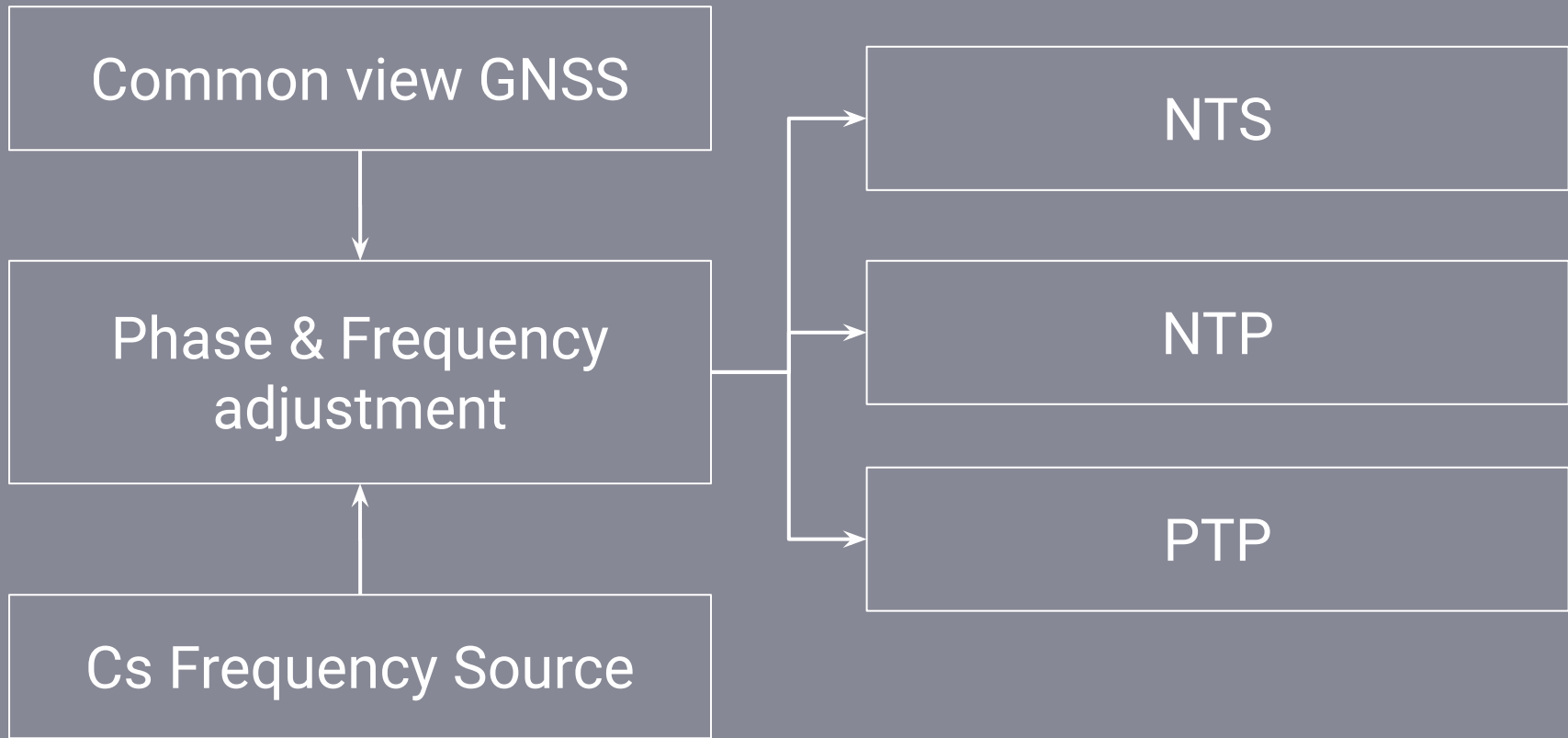


- Signal propagation time:  $\delta$
- Additionally:
  - Variation in propagation time
  - Asymmetry in propagation time









# Nodes

- Stockholm
  - Two locations
- Malmö
- Gothenburg
- Sundsvall
- Luleå









← Arista 7130L NTS FPGA

← Measurement- and web servers

← NTP Servers

← PTP and GNSS

← Frequency distribution

← Frequency measurement

← Frequency amplifier

← Frequency and phase adjustment

← Frequency generator (Cs)

SP.UTC-STH\_CS1 foffset estimated +5.04427e-13 foffset applied: -507e-15 111123CF

Symmetricon

5071A

PRIMARY FREQUENCY STANDARD

07 59 20

■ Attention

■ Continuous  
Operation

STH\_CS01

TIMETECH



Time Interval Counter

2015/12/11 09:33:58 NTP1 Slit: 9999...99  
disabled d: 0.000ns

+, +, +, +, Enter, ESC, Menu, Local

Power  
+5V  
-5V  
Error  
Oper.

mctic1

27

28

29

SDI  
SPECTRADYNAMICS

Monitor  
AC Power DC Power 1 PPS 5 MHz 10 MHz

CSDA-1  
CLOCK SIGNAL DISTRIBUTION  
AMPLIFIER

csda1

30

31

SDI  
SPECTRADYNAMICS

ON DATA STATUS

RS-232

Frequency Offset (Hz)  
0  
Phase Offset (deg)  
0  
FREQ PHASE TIME SET HELP

FREQUENCY AND PHASE OFFSET GENERATOR 10G-5

REFERENCE INPUTS  
Signal PLL Lock 1 PPS  
5 MHz In 1 PPS In  
OUTPUTS  
5 MHz Out 1 Signal 5 MHz Out 2  
1 PPS Out 1 1 PPS 1 PPS Out 2

32

33

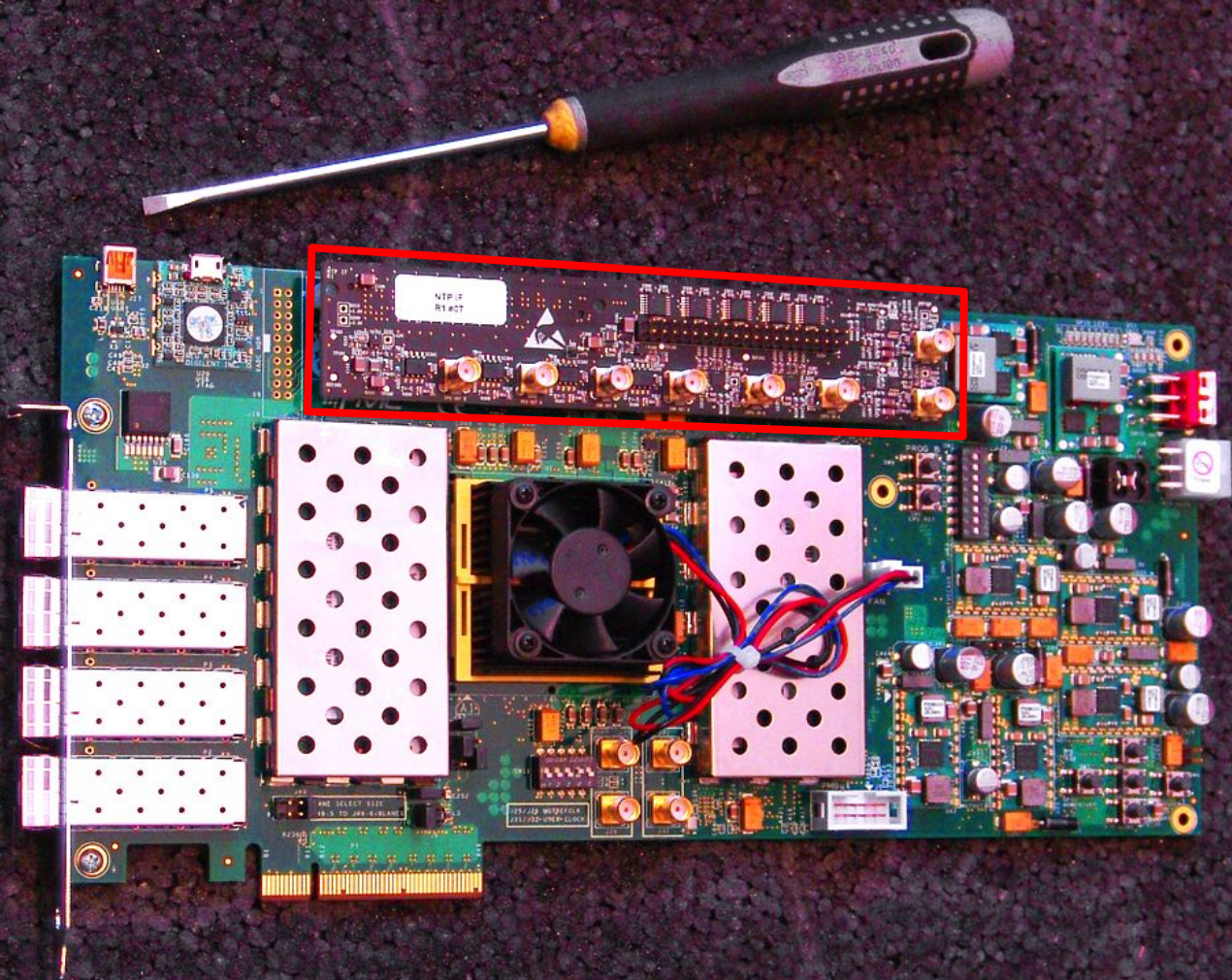
34

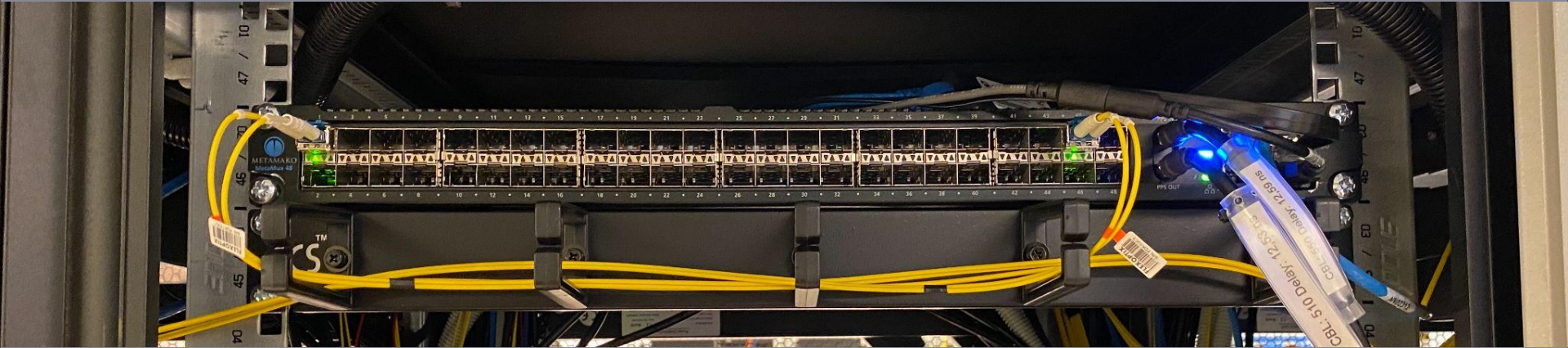


CBL: 222, Delay: 6,21 ns

CBL: 208, Delay: 6,17 ns

CBL: 221, Delay: 6,21 ns





Netnod/FPGA\_NTP\_SERVER: # x

github.com/Netnod/FPGA\_NTP\_SERVER

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About

A FPGA implementation of the NTP and NTS protocols

fpga verilog fpga-ntp-server

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Releases 2 tags

Packages No packages published

Contributors 3

secworks Joachim Strömbergson

wingel Christer Weinigel

mechmen Rolf Andersson

Languages

Verilog 63.2% Python 16.4% C 14.3% Makefile 2.8% Tcl 2.7% Shell 0.4% SystemVerilog 0.2%

wingel Merge pull request #1 from Assured/master d2f1d83 on 23 Sep 2021 425 commits

Doc	First set for upload to github	6 years ago
FPGA	Move most of top level README.md into FPGA/targets/ntps_vc709.	13 months ago
Linux_Driver	Use same MAC addresses as legacy_ntp	14 months ago
.gitignore	Make git ignore bitstream files.	16 months ago
.gitmodules	Move rosc_entropy to cores	17 months ago
LICENSE	Update copyright statement with Netnod + BSD-3 clause	13 months ago
README.md	Minor edits to fix spelling, language.	7 months ago

README.md

## FPGA\_NTP\_SERVER

### Introduction

This repository contains the source code for a complete, FPGA based hardware implementation of a Network Time Protocol (NTP) server. The implementation includes hardware support for [Network Time security \(NTS\)](#).

The server implements the complete network stack in hardware, which allows high performance, low latency and low jitter. The design supports scalability through parallel, independent network engines.

The repository contains setup and build targets to implement the server on existing FPPGA boards. The currently supported FPGA boards ar:

- [Xilinx VC709 Connectivity Kit](#). A reference board with a Virtex 7 FPGA device.
- [Xilinx VCU-118 Evaluation Kit](#). A reference board with a Virtex Ultrascale+ FPGA device.

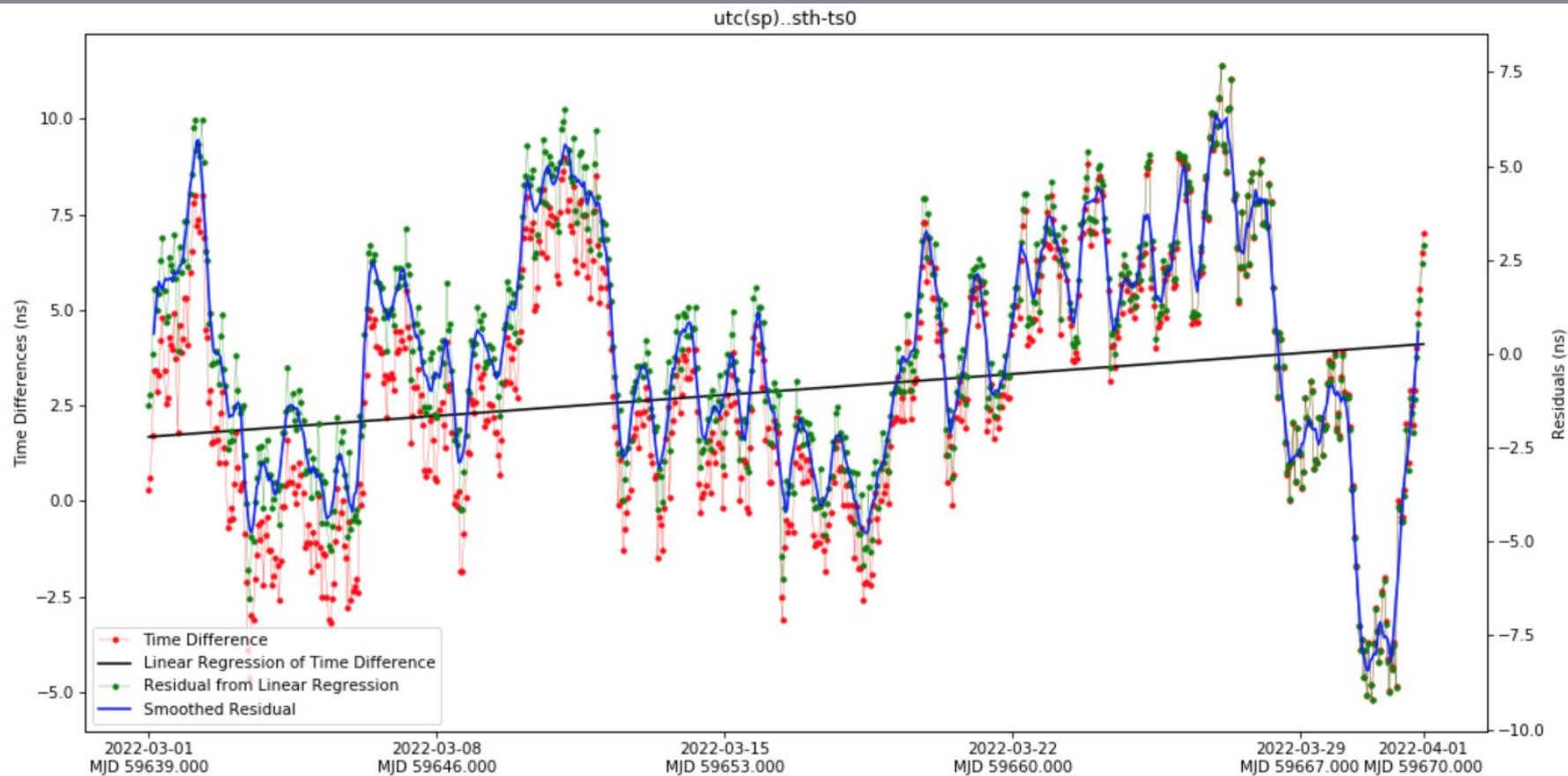
Look at README.md in the respective target directories for more information on how to build an FPGA image and for the two FPGA reference boards. The VC709 project has the most complete instructions on how to use it, the VCU118 project lacks documentation on how to set up the hardware, but is fairly similar.

### Status

The design is complete, verified and tested in real hardware and systems. The server is used to operate the [Swedish Distributed Time Service](#).

NET NOD

# New: Time offset +/- $1 \times 10^{-8}$ , or 10ns





# Recommendations

- **Ensure you know what time it is**
  - Measure frequency and phase errors
- **Get time and frequency from multiple sources**
  - Compare them with each other
- **Know the stability of the oscillator you use**
  - Make a risk assessment of errors
  - Compare with acceptable errors

# References

- **From Sundials to Atomic Clocks: Understanding Time and Frequency**
  - Jespersen, James and Jane Fitz-Randolph, (<http://tf.nist.gov/general/pdf/1796.pdf> – 26 MB, 306 pages) 2nd (revised) edition, Mineola, New York: Dover Publications, 1999 ISBN 0-16-050010-9
- **Longitude: The True Story of a Lone Genius Who Solved the Greatest Scientific Problem of His Time**
  - Dava Sobel 1995, Walker Publishing Company, Inc., New York, ISBN 0-8027-1312-2
- **Market-driven Challenges to Open Internet Standards**
  - Global Commission on Internet Governance. Centre for International Governance Innovation and Chatham House. GCIG Paper No. 33. Patrik Fältström, May 20 2016